REMARKS

Applicant hereby submits this response to the communication dated July 26, 2006 which indicated that the response to the prior office action was not fully responsive in that it failed to properly address the Examiner's section 112 rejections. Accordingly, Applicant re-submits the prior response with additional explanation concerning the section 112 rejections. In the office action dated November 1, 2005, the Examiner indicated that claims 4, 8 and 9 were rejected under section 112, first paragraph as failing to comply with the written description requirement in that the claims contained subject matter which was not described in the specification. Specifically, the Examiner asserted there is no support for the negative limitation that there are no electrical conductors opposite the side where all electrodes are formed. Applicant respectfully submits that the assertion of the Examiner is erroneous in that Figure 1 K and the corresponding written description on page 20 clearly illustrates individual chip members 4 which are described as being non-defective LSI chips that are rearranged and contained in the pseudo wafer 24.

The specification indicates that the chips 4 of the pseudo-wafer are diced again into discrete chips by cutting through the portion of the insulating film 6 which covers the side walls of the LSI chips using the dicing blade 9 or a laser beam. See specifically the Applicant's disclosure at page 20 in lines 22-27. Applicant respectfully submits that the drawing very clearly illustrates bump electrodes formed on a single side of the chip and that the resin material or insulating material at the side walls thereof 6 is located on 4 sides of the chip. As illustrated in Figures 1C-1D, the side opposite the side of the chips 4 wherein the electrodes are located is ground down to a common level as shown in Figure 1D as also verbally described in the specification. Accordingly, in light of the foregoing, Applicant respectfully submits that

there is more than ample support for the claimed invention as now specified. The undersigned invites the Examiner to contact him directly should the Examiner have any additional questions concerning this matter.

In response to the Examiner's final office action dated November 1, 2005, Applicant hereby presents a Request for a Continued Examination so that the Examiner may consider the claims as modified herein. More specifically, Applicant has modified the independent claims to specify that the side of the chip members opposite the side at which the electrodes are located which has been grinded to a common level is secured to a dicing sheet. Advantageously, the specified structure enables the manufacture of electrical connection structures such as solder balls to be formed exclusively on non-defective semiconductor chips. This desirably decreases the manufacturing costs because defective chips are not processed to the point at which electrical interconnection structures are formed.

Applicant respectfully submits that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's presently claimed invention. More specifically, Applicant notes that the reference upon which the Examiner had relied in rejecting the claims under 35 USC section 102 is actually directed to a much different technology. More specifically, the cited reference, United States patent number 5,841,193 is actually directed to a technique for manufacturing a multi--chip module wherein the various semiconductor chips are interconnected. This is in sharp contrast with the present invention wherein the intermediate structure is secured to a dicing sheet so that the individual chips may be separated from the pseudo-wafer.

For example, the abstract of this reference notes that the multichip module comprises a plurality of chips affixed in a planar array by a structural material which surrounds the sides

of the chips such that the upper surfaces of the chips and an upper surface of the structural material are co-planar and the lower surface of at least one chip and a lower surface of the structural material are co-planar. A photo-patternable dielectric is disposed directly on the upper surfaces of the chips. The photo-patternable dielectric includes vias to at least some contact pads at the upper surfaces of the chips and the module further comprises an intrachip metallization layer on the photo-patternable dielectric layer. Subsequent processing provides a multi-layer chip interconnect structure over the intrachip metallization layer and photo-patternable dielectric. Testing and repair of the module can be accomplished prior to or subsequent to fabrication of the multi-layer chip interconnect. Formation of multiple single chip modules is accomplished by singulating the multichip module into individual packages.

In light of the foregoing, Applicant respectfully submits that there is no teaching or suggestion in the cited reference concerning the use of a dicing sheet as now specified in the claims. Accordingly, in light of the foregoing, Applicant respectfully submits that all claims now stand in a condition for allowance.

Respectfully submitted,

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